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(54) Process for the manufacturing of a SOI wafer by oxidation of buried cavities

(57) The process comprises the steps of forming, in a wafer (200) of monocrystalline silicon, first trenches extending between portions of the wafer; etching the substrate (90) to remove the silicon around the first trenches and forming cavities (121) in the substrate (90); covering the walls of the cavities with an epitaxial growth inhibiting layer; growing a monocrystalline epitaxial layer (126) on top of the substrate (90) and the cavities so as to obtain a monocrystalline wafer embedding buried cavities completely surrounded by silicon; forming second trenches (144) extending in the epitaxial layer (126) as far as the cavities; removing the epitaxial growth inhibiting layer; oxidizing the cavities, forming at least one continuous region (127) of buried oxide; depositing a polysilicon layer on the entire surface of the wafer and inside the second trenches (144); removing the polysilicon layer on the surface, leaving filling regions (148) inside the second trenches (144); oxidizing, on the top, portions of said filling regions so as to form field oxide regions (150).

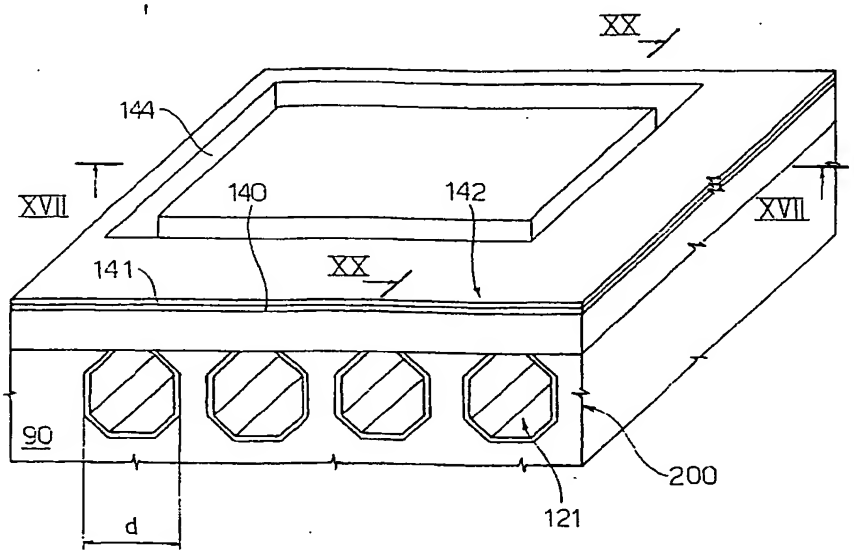

Fig. 16

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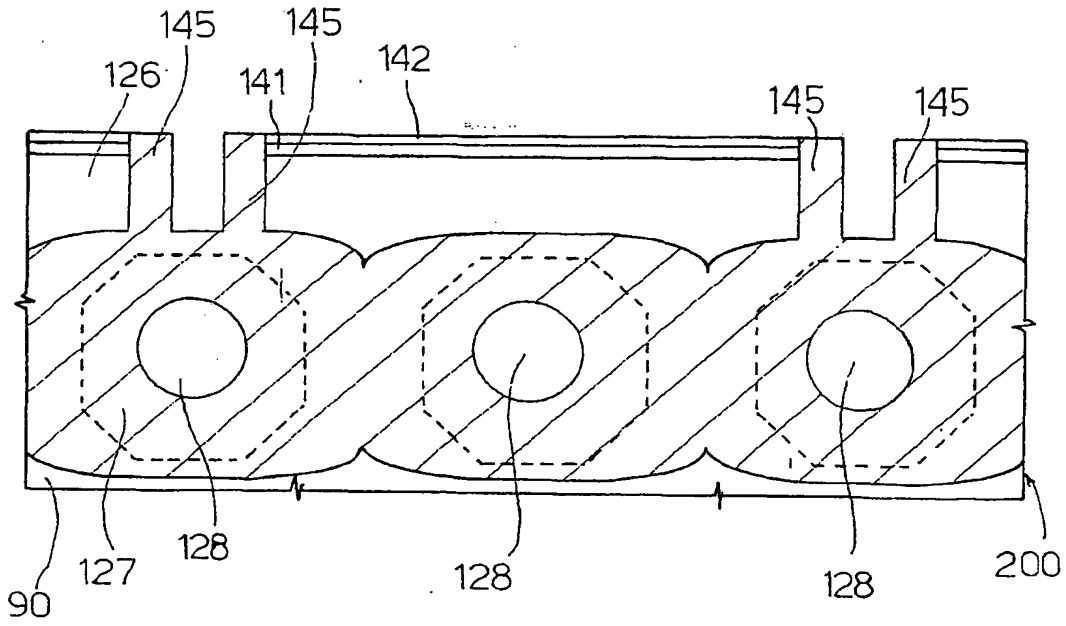


Fig.18

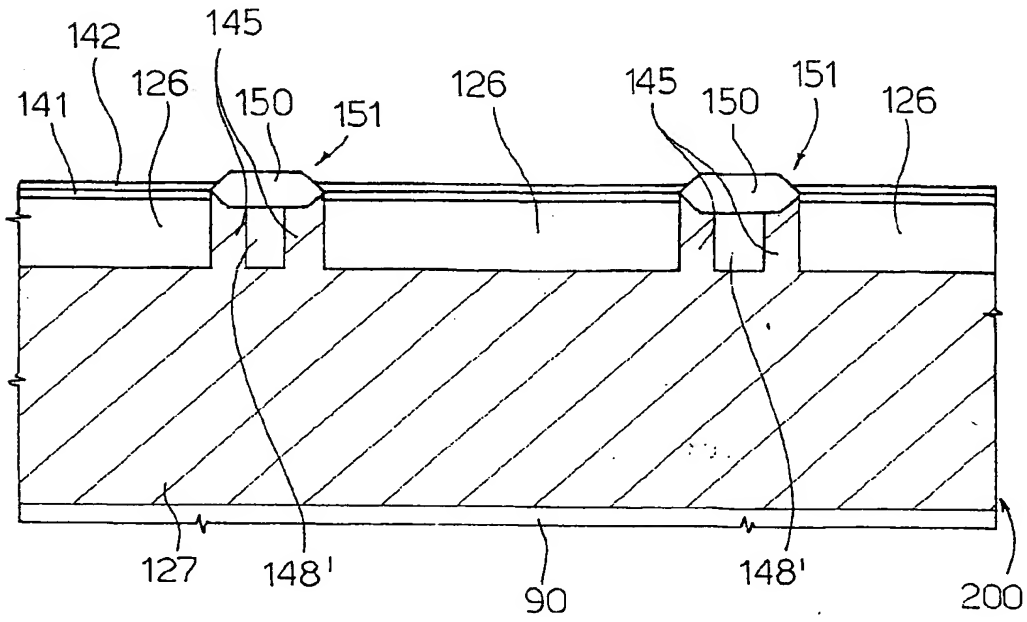


Fig.22

Description

[0001] The present invention regards a process for the manufacturing an SOI wafer by oxidation of buried channels.

[0002] As is known, according to a solution currently very widespread in the microelectronics industry, the substrate of integrated devices is obtained from monocrystalline silicon wafers. In the last few years, as an alternative to just silicon wafers, composite wafers have been proposed, so-called "SOI" (Silicon-on-Insulator) wafers comprising two silicon layers, one of which thinner than the other, separated by a silicon oxide layer.

[0003] A process for manufacturing SOI wafers is the subject of European patent application No. 98830007.5, filed on 13 1.98 in the name of the present applicant, and is described hereinafter with reference to Figures 1 to 8.

[0004] According to this process, on a surface 3 of a substrate 2, a first silicon oxide layer is initially grown having a thickness of between, for example, 20 and 60 nm. A first silicon nitride layer having a thickness of between 90 and 150 nm is then deposited. Using a resist mask, dry etching is carried out on the uncovered portions of the first oxide layer and the first nitride layer, and the resist mask is then removed, providing the intermediate structure of Figure 1, where the wafer thus obtained is indicated, as a whole, by 1, and the portions of the first oxide layer and of the first nitride layer that have remained after dry etching are indicated by 4 and 5, and define respective first protective regions 7 covering first portions 8' of the substrate 2.

[0005] The first protective regions 7 form a hard mask, indicated as a whole by 9, which is used to etch the substrate 2 at second portions 8" left uncovered by the mask 9, so as to form initial trenches 10 (Figure 2). Subsequently, as shown in Figure 3, the wafer 1 is subjected to oxidation, to form a second oxide layer 11 which has a thickness of between, for example, 20 and 60 nm and covers the walls and the bottom of the initial trenches 10, and then a second silicon nitride layer 12 is deposited for a thickness of between 90 and 150 nm.

[0006] Next, layers 12 and 11 are anisotropically etched without mask. Given the anisotropy of the etching, the horizontal portions of the second silicon nitride layer 12 and second silicon oxide layer 11 on the bottom of the initial trenches 10, and the portion of the second silicon nitride layer 12 above the portions 4 and 5 are removed, providing the intermediate structure of Figure 4, wherein the regions 8' are still covered on top by the mask 9 and on the sides (i.e., on the vertical walls of the initial trenches 10) by a silicon oxide portion 11' and by a silicon nitride portion 12'. Instead, the substrate 2 is bare on the bottom 15 of the initial trenches 10.

[0007] The uncovered silicon at the bottom 15 of the initial trenches 10 is then etched away, to deepen the initial trenches 10 themselves until final trenches 16 having a desired depth are obtained. In particular, the depth of the final trenches 16 determines the dimensions of the desired buried oxide layer, and hence the electrical characteristics of the SOI wafer, as will be described more clearly hereinafter, and consequently the depth is determined according to the specifications provided for the final SOI wafer.

[0008] The substrate 2 now comprises a base portion 2', and a plurality of "columns" 18 which extend vertically from the base portion 2'. The intermediate structure of Figure 5 is thus obtained, wherein the silicon nitride portions 5 and 12' are no longer distinct from one another and are designated by 19. The silicon oxide portions 4 and 11' are no longer distinct from one another and are designated by 20 and form, together with portions 19, second protective regions 30.

[0009] A thermal oxidation step is then carried out, so that the exposed silicon regions of the columns 18 are transformed into silicon oxide. In practice, oxide regions are gradually grown at the expense of the silicon regions, starting from the side walls of the final trenches 16 towards the inside of the columns and partly also towards and within the base portion 2'. Since during oxidation there is an increase in volume, the oxide regions being formed gradually occupy the space of the final trenches 16 until they fill the trenches completely and join up together. The oxidation step terminates automatically once the columns 18 are completely oxidised (except for the top area or tip, designated by 21, which is protected by the second protective regions 30), thus forming a continuous buried oxide region 22, shown in Figure 6, where the vertical continuous lines indicate the meeting surfaces of the oxide regions being formed from the walls of two adjacent final trenches 16, to highlight the expansion of the oxide.

[0010] Subsequently, by selective etching, the second protective regions 30 are eliminated so as to uncover the tips 21, which form the germs for a subsequent epitaxial growth.

[0011] The structure of Figure 7 is obtained, showing the three-dimensional structure of the wafer 1 in this step. Next, an epitaxial growth is performed, the parameters of which are chosen to as to prevent nucleation of the silicon in the areas overlying the buried oxide region 22, and a high ratio of lateral to vertical growth is chosen so as to obtain first a horizontal growth of the silicon around the tips 21 (and thus the coating of the top surface of the buried oxide region 22), and subsequently the vertical growth of an epitaxial layer 23. After an optional step of chemical-mechanical polishing to planarize the top surface of the wafer 1, the final structure of the wafer 1 is then obtained, as shown in Figure 8.

[0012] Thereby, an SOI wafer can be produced using only process steps that are common in microelectronics, with much lower costs than those of processes currently used for forming SOI substrates.

[0013] The above described manufacturing process has, however, the drawback that the shape of the buried oxide region 22 is not ideal. In fact, as highlighted in the

enlarged detail of Figure 9, during thermal oxidation, the exposed silicon regions of the columns 18 are oxidised along curved lines, so that the buried oxide region 22 presents, underneath, a shape that is defined by a series of arches 35 and, on top, a shape defined by a series of cusps 37 extending upwards at each wall of the final trenches 16. In addition, between the grown epitaxial silicon layer and the buried oxide layer, a void area 40 is present. This shape of the buried oxide region 22 renders critical the epitaxial growth of the silicon to form the SOI wafer, and, in addition, the void area 40 is a cause of non-optimal electrical characteristics.

[0014] The aim of the present invention is therefore to overcome the drawbacks of the manufacturing process described above.

[0015] According to the present invention, a process for manufacturing SOI wafers and a SOI wafer are provided, as defined in Claim 1 and in Claim 14.

[0016] For a better understanding of the present invention, a preferred embodiment thereof will now be described, purely as a non-limiting example, with reference to the attached drawings, wherein:

- Figures 1-6 show cross-sections through a SOI wafer in successive manufacturing steps according to a prior process;
- Figures 7 and 8 show perspective cross-sections in two subsequent steps of the prior manufacturing process;
- Figure 9 shows a detail of Figure 6, in enlarged scale;
- Figures 10-15 show cross-sections through a SOI wafer corresponding to the manufacturing process according to the present invention;
- Figure 16 shows a perspective cross-section in a subsequent step according to the present invention;
- Figures 17-18 show cross-sections of the wafer of Figure 16, taken along the plane XVII-XVII, in subsequent steps of the manufacturing process according to the present invention;
- Figures 19-22 show cross-sections of the wafer of Figure 16, taken in a plane XX-XX, in successive steps of the manufacturing process according to the present invention; and
- Figure 23 shows a cross-section similar to that of Figure 22, in reduced scale.

[0017] The invention will now be described with reference to Figures 10-23.

[0018] According to Figure 10, on the surface 211 of the wafer 200 of semiconductor material comprising a monocrystalline substrate 90, a first oxide layer having a thickness of, for example, between 20 and 60 nm is grown. A first nitride layer having a thickness of between 90 and 150 nm is then deposited. Using a resist mask, the uncovered portions of the first nitride layer and of the first oxide layer are dry etched, and the resist mask is then removed. In this way, the portions of the first oxide layer and of the first nitride layer that are left after dry etching (oxide portions 112 and nitride portions 113 in Figure 10) form a hard mask, designated as a whole by 114.

[0019] Subsequently, using the hard mask 114, the wafer 200 is anisotropically etched (first trench etch) to form first trenches 115 (Figure 11) having a width of, for example, between 1 and 3 μm (preferably, 2 μm) and a depth depending onto the structures to be made, for example 10-30 μm.

[0020] Next (see Figure 12), timed etching in TMAH (tetramethyl ammonium hydroxide) of the silicon around the first trenches 115 is carried out. Since this etch is basically of an isotropic type, it enables the formation of cavities 121 having a width d (in the widest point) of, for example, 10-200 μm and, in any case, much greater than the first trenches 115. Typically, the first trenches 115 have a shape elongated in the direction perpendicular to the plane of the drawing, and the cavities 121 form elongated channels.

[0021] According to the orientation and duration of the TMAH etch, it is possible to obtain, in a known way, different geometries of the cavities 121. In particular, in the case of elongated cavities 121 extending lengthwise at 90° with respect to the flat of the wafer, i.e., perpendicular to the sheet of the drawing, the cavities 121 have the shape shown in Figure 12. In the case of elongated cavities 121 extending lengthwise at 45° to the flat of the wafer, the cavities 121 have the shape of tubs with approximately vertical walls extending from underneath the hard mask 114.

[0022] Next (Figure 13), the walls of the cavities 121 are coated with an inhibiting layer 122, which does not allow epitaxial growth. For this purpose, for example, a fast oxidation step may be performed so as to grow an oxide layer (having a thickness greater than the portions of oxide 112 and nitride 113 which cover the surface 211 of the wafer 200 and the walls of the first trenches 115, as explained later, for instance between 60 and 200 nm); in the alternative, a conform layer of a material chosen from among deposited oxide, nitride, and tetraethyl orthosilicate (TEOS) may be deposited.

[0023] Next (Figure 14), the hard mask 114 is removed from the surface 211 of the wafer 200. During removal of the oxide portion 112 and nitride portion 113, also part of the inhibiting layer 122 is removed; however, since the latter is thicker, it is not removed completely and remains to an extent sufficient to ensure complete covering of the walls of the cavities 121.

[0024] Subsequently (Figure 15), epitaxial growth is carried out, using as germ the monocrystalline silicon of the substrate 90. Consequently, the monocrystalline silicon grows, starting from the surface 211, both vertically and horizontally so as to close the cavities 121. The silicon does not grow, instead, inside the cavities 121, given the presence of the inhibiting layer 122. In this way, a monolithic wafer 200 of monocrystalline silicon (shown in Figure 15) is obtained, comprising the substrate 90

and an epitaxial layer 126, and housing completely closed cavities 121 internally delimited to a large extent by the inhibiting layer 122.

[0025] As shown in Figures 16 and 17, a trench etch (second trench etch) of the silicon overlying the cavities 121 is then carried out to form second connection trenches, for example having the shape of a closed-path line extending roughly along the external perimeter of the region of the substrate 90 that houses the cavities 121. For this purpose, in a per se known manner, a third oxide layer 140 is initially deposited or grown; then, a third nitride layer 141 (Figure 16) is deposited. The third oxide layer 140 and third nitride layer 141 are defined photolithographically so as to form a second hard mask 142 which covers the wafer 200 completely, except for the parts of the epitaxial layer 126 that are to be etched. The uncovered silicon is then etched to form second trenches 144, which extend up to the cavities 121.

[0026] Subsequently, thermal oxidation is carried out so that the silicon regions exposed around the cavities 121 and on the walls of the second trenches 144 transform into silicon oxide. In practice, there is a gradual growth of the oxide regions at the expense of the silicon regions, starting from the side walls of the cavities 121 and of the trenches 144 towards the inside of the cavities and trenches themselves and in part also outwards. Since during the oxidation there is an increase in volume, the oxide regions being formed gradually occupy the space of the cavities 121 until they close the cavities almost completely and join up together. The oxidation step is completed once the cavities are oxidised (possibly apart from an internal area where a hole, designated by 128, is left), thus forming a continuous buried oxide region 127 - shown in Figures 18 and 19, which are taken along two perpendicular planes - whereas oxide regions 145 are formed on the side walls of the trenches 144.

[0027] Next, a polysilicon layer 148 is deposited on the surface of the wafer 200 and fills the trenches 144, as shown in Figure 20.

[0028] Subsequently, by etching or a mechanical process, the polysilicon layer 148 is removed from the surface of the wafer 200 and remains only inside the trenches 144, where it forms filling regions 148', as shown in Figure 21.

[0029] Finally, the upper portions of the filling regions 148' are thermally oxidised so as to form field oxide regions 150 which close the filling regions 148' at the top and in a complete way, forming, together with the oxide regions 145 and the filling regions 148' themselves, insulating regions 151, as shown in Figure 22.

[0030] The advantages of the described process are the following: the present process makes it possible to obtain a SOI wafer wherein the epitaxial monocrystalline silicon layer is completely passivated by the continuous buried oxide region 127, because the void area between the oxide and the epitaxial monocrystalline silicon (designated by 40 in Figure 9) is no longer present, thereby reducing the risk of recombination between charge carriers in this area. The described process does not require additional masks as compared to the processes comprising trench insulation, since the second hard mask 142 required for forming the second trenches 144 can be obtained simply by modifying the trench mask already envisaged in the known processes.

[0031] Furthermore, the cavities 121 may extend over the entire wafer area, and in this case also the continuous buried oxide region 127 extends along the entire wafer.

[0032] Alternatively, the cavities 121 may occupy only partially the wafer area, so as to obtain, in the wafer, signal areas, wherein a completely isolated epitaxial silicon region is designed to house signal processing electronic devices and oxide-free power areas (with high thermal conductivity) designed to house power devices in which the epitaxial layer is directly and electrically connected to the substrate 90. For example, it is possible to manufacture wafers like the one shown in Figure 23, wherein a signal area 160, insulated by the continuous oxide region 127 and the insulating region 151, and a power area 161 are shown. Figure 23 also shows an N+-type buried layer 155, obtained by an antimony implant in the starting substrate 90, before the cavities 121 are formed. After the growth of the epitaxial layer 126, the doping agents spreads also in the latter layer.

[0033] Finally, it is evident that numerous modifications and variations may be made to the process and device described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims.

Claims

1. A process for manufacturing an SOI wafer (200), characterized, in sequence, by the steps of:

   - forming cavities (121) in a substrate (90) of semiconductor material;
   - growing an epitaxial layer (126) of monocrystalline type on top of said substrate (90) and said cavities (200) to obtain a wafer (200) of monocrystalline semiconductor material embedding said cavities (121), said cavities being completely surrounded by said monocrystalline material; and
   - oxidizing said cavities to form at least one continuous region (127) of buried oxide.

2. The process according to Claim 1, characterized in that said step of forming cavities (121) comprises the steps of:

   - forming first trenches (115) in said substrate (90); said first trenches extending between portions of said wafer; and

- etching said substrate (90) to remove said semiconductor material around said first trenches (115).

3. The process according to Claim 2, characterized in that said etching step is carried out in TMAH.

4. The process according to Claim 3, characterized in that said etching step is time-controlled.

5. The process according to any of Claims 2-4, characterized in that said step of forming first trenches (115) comprises the steps of:

- forming a first hard mask (114) of insulating material; and
- anisotropically etching said substrate (90), using said first hard mask.

6. The process according to any of the foregoing Claims, characterized in that, after said step of forming said cavities (121), the step is carried out of coating walls of said cavities with a layer inhibiting epitaxial growth (122).

7. The process according to any of Claims 1-6, characterized in that, before said step of oxidizing, the step is carried out of forming second trenches (144) extending in said epitaxial layer (126) up to said cavities (121).

8. The process according to Claim 7, characterized in that said step of forming second trenches (144) comprises the steps of forming a second hard mask (141, 142) and of etching said epitaxial layer (126).

9. The process according to Claim 7 or Claim 8, characterized in that it further comprises the steps of:

- filling said second trenches (144) with filling regions (148') of semiconductor material; and
- oxidizing upper portions (150) of said filling regions so as to form regions (126) of monocrystalline epitaxial silicon that are insulated at the sides and at the bottom.

10. The process according to Claim 9, characterized in that said step of filling said second trenches (144) comprises the steps of:

- depositing a semiconductor material layer (148) over the entire surface of the wafer; and
- removing said semiconductor material layer (148) on said surface of said wafer.

11. The process according to any of the foregoing Claims, characterized in that said cavities (121) extend along the entire area of said wafer (200).

12. The process according to any of Claims 1-10, characterized in that said cavities (121) extend only on a part of the area of said wafer (200).

13. The process according to any of the foregoing Claims, characterized in that, before said first step of forming first trenches, the step is carried out of doping said substrate (90) of semiconductor material.

14. An SOI wafer of semiconductor material, comprising a substrate (90) of monocrystalline semiconductor material, at least one semiconductor material region (126) having a monocrystalline structure, and an insulating material layer (127) arranged between said at least one semiconductor material region and said substrate, further characterized by:

trenches (144) having walls covered with dielectric material a layer (145) and housing filling portions (148') of semiconductor material, said trenches delimiting at the sides said at least one semiconductor material region; and
field oxide regions (150) overlying at the top said filling regions (148').

15. The SOI wafer according to Claim 14, characterized in that said semiconductor material region (126) has a first doping level and in that the wafer comprises conductive regions (155) of semiconductor material arranged between said semiconductor material region (126) and said insulating material region (127) and having a second doping level higher than said first doping level.

16. The SOI wafer according to Claim 14 or 15, characterized by an epitaxial region (126") directly overlying said substrate (90) and surrounding, at least on one side, said semiconductor material region (126') and part of said insulating material region (127).

Fig.1

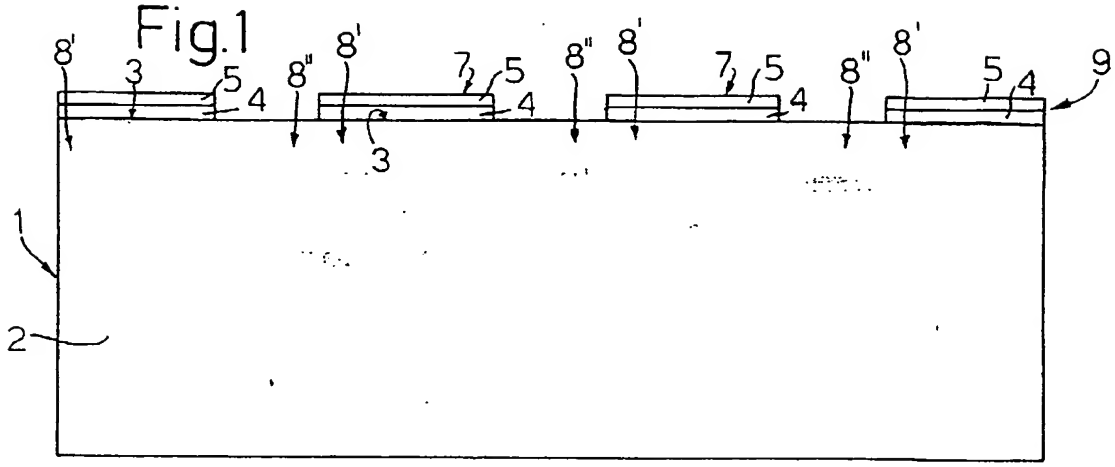


Fig.2

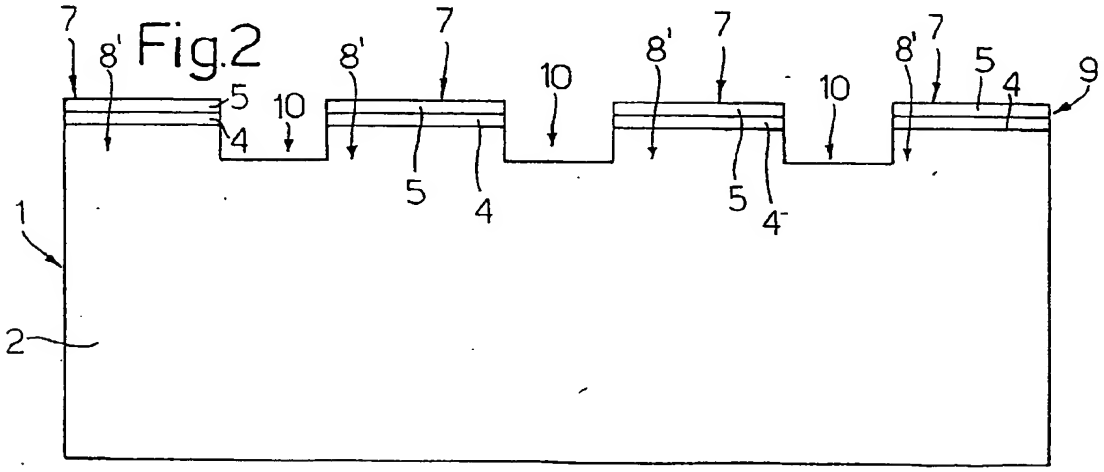


Fig.3

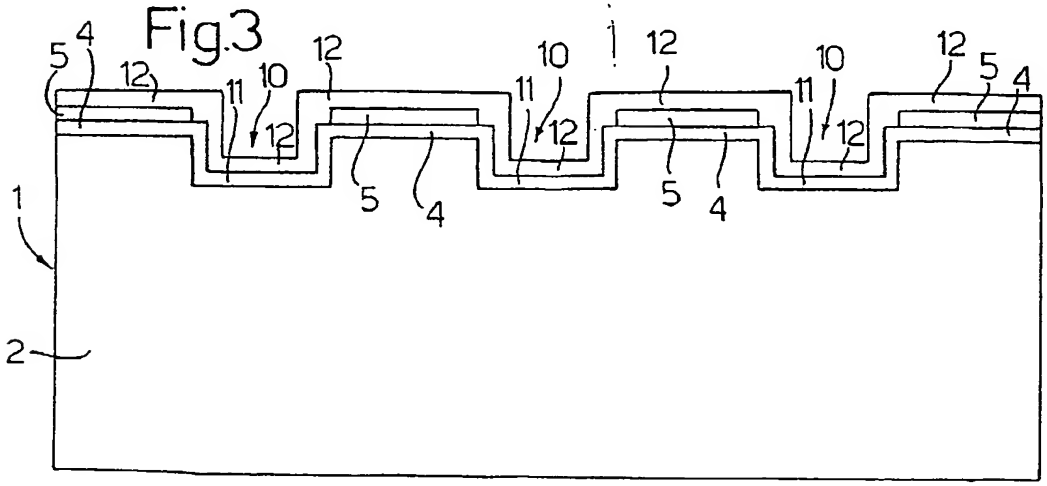


Fig.4

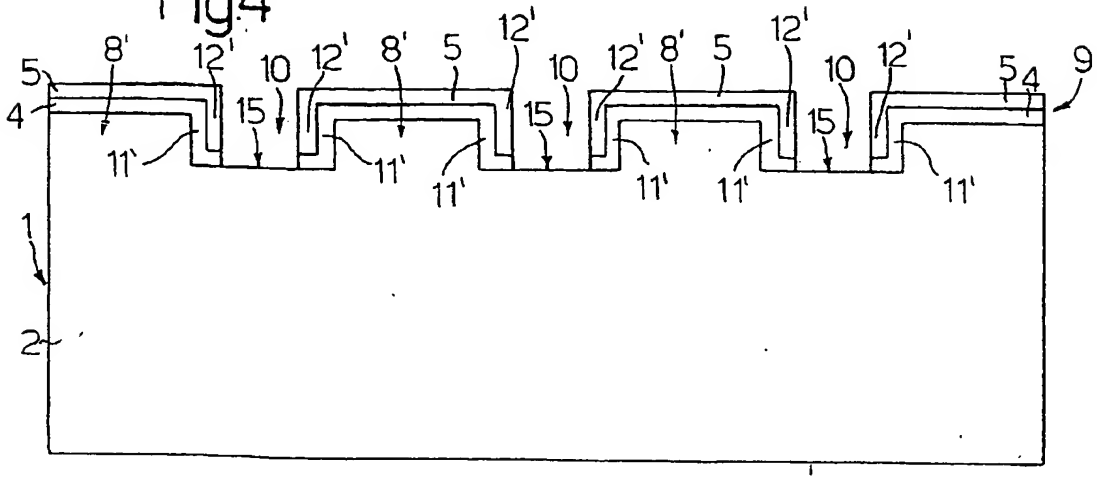


Fig.5

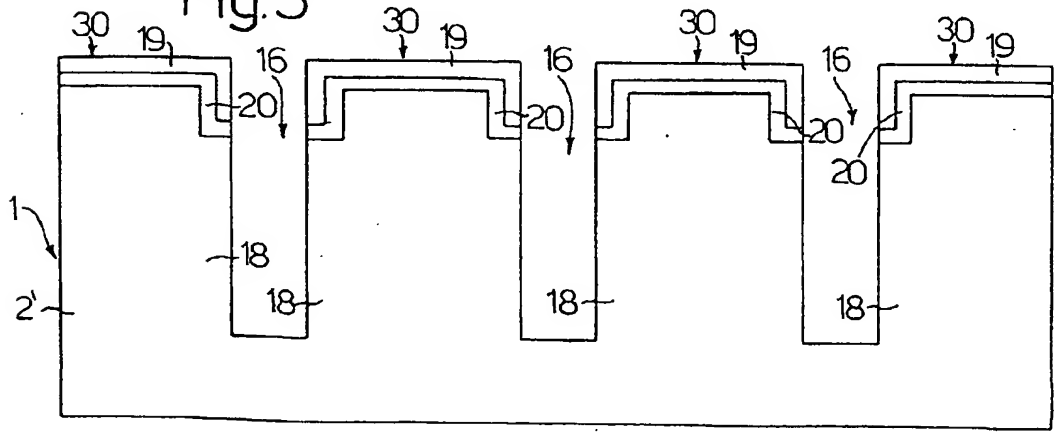
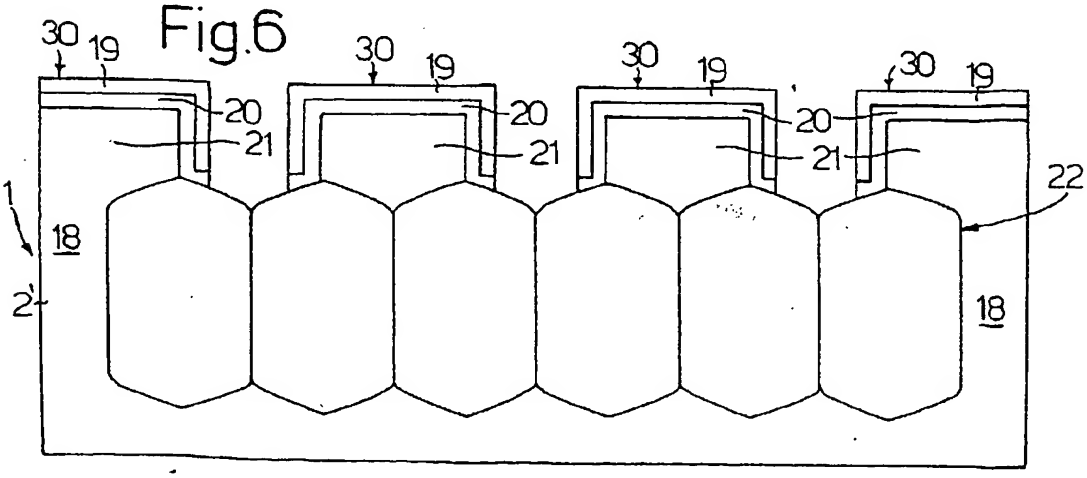


Fig.6



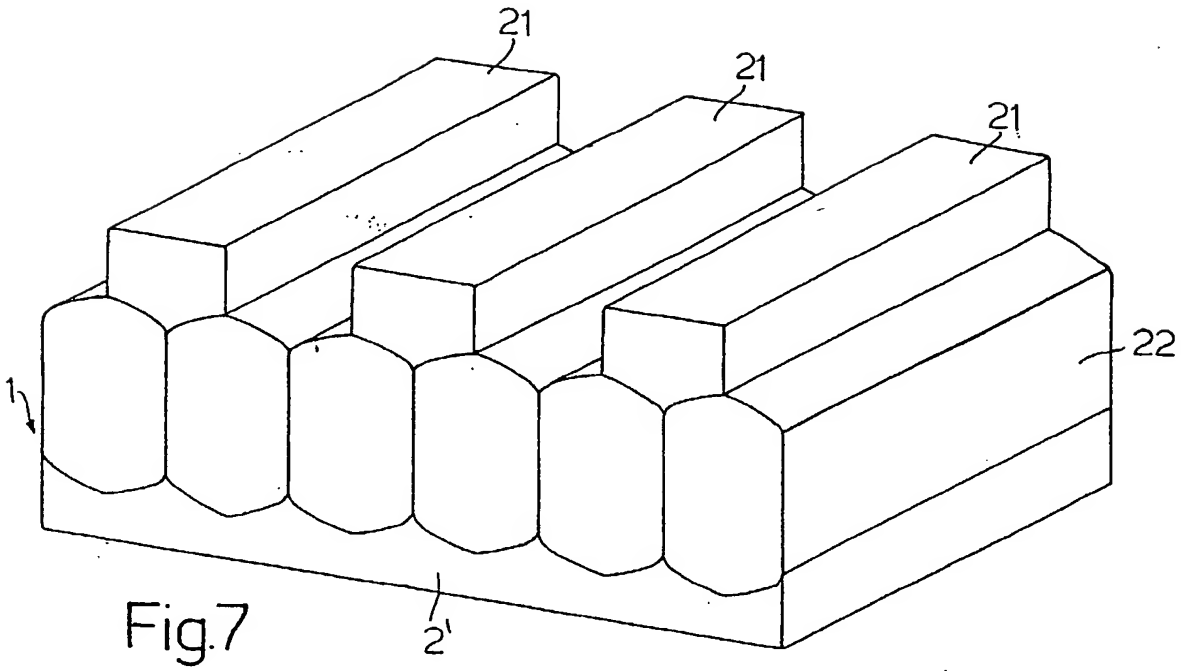


Fig.7

Fig.8

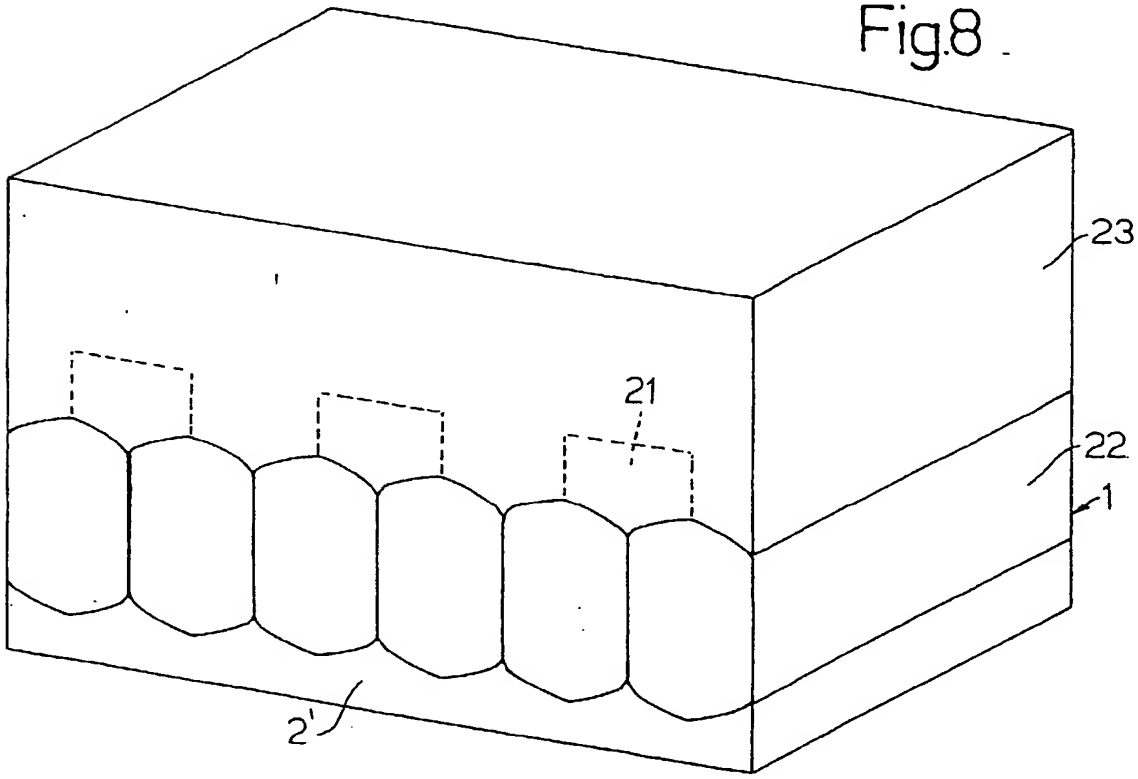


Fig.9

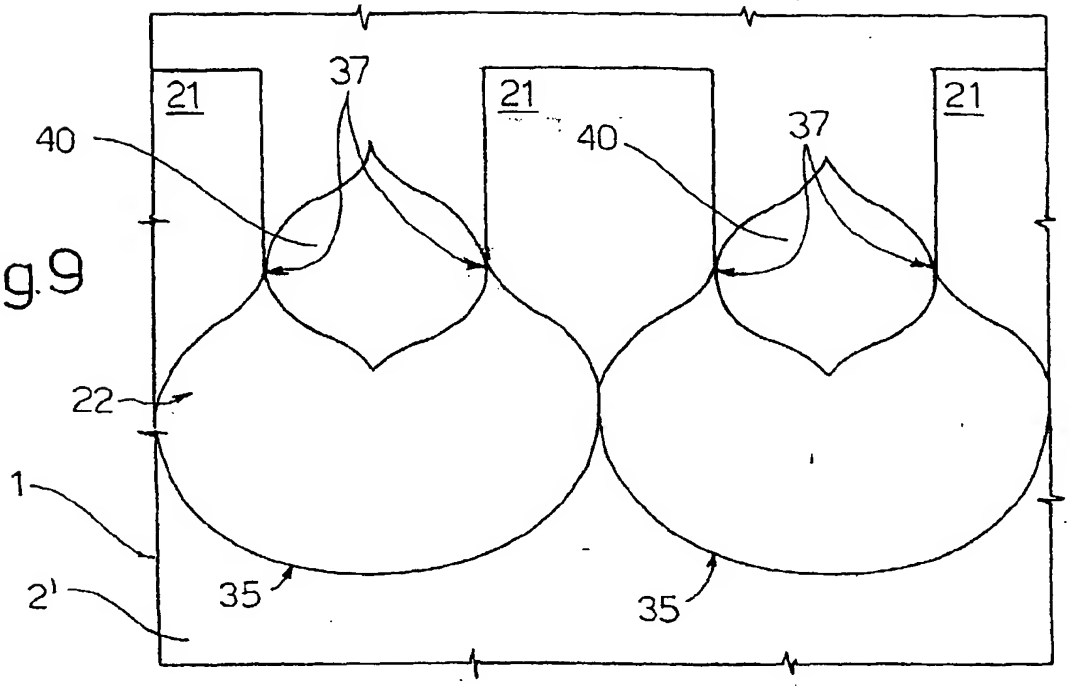
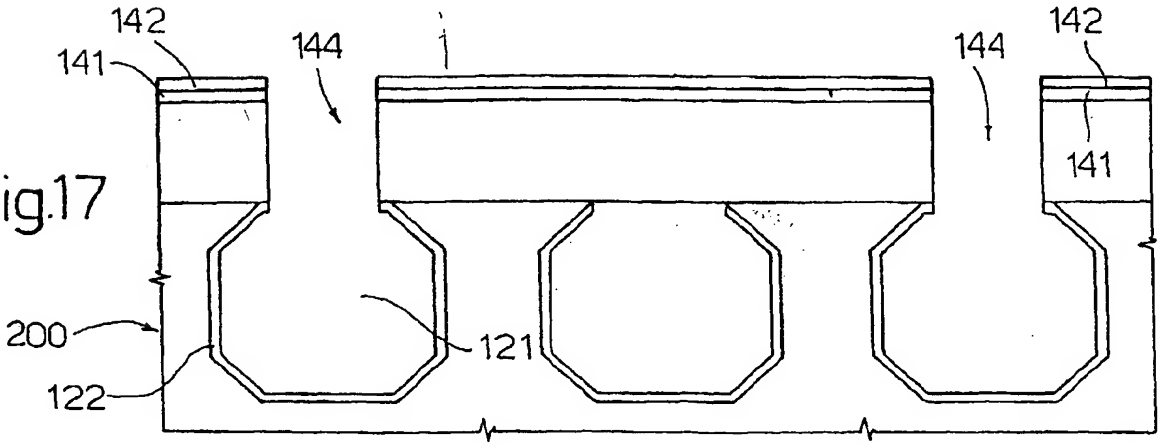


Fig.17



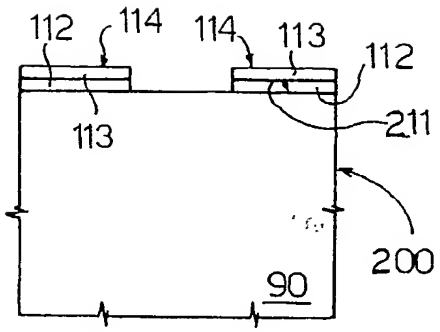


Fig.10

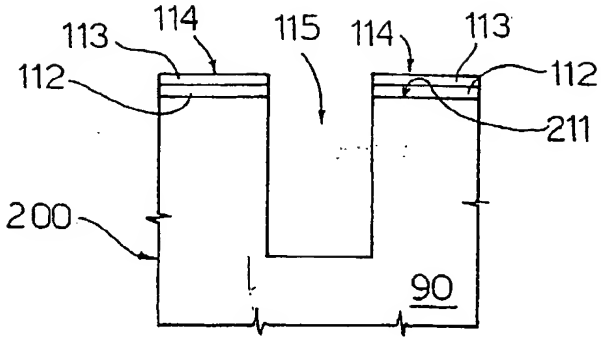


Fig.11

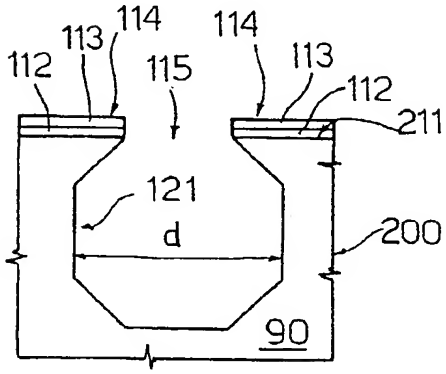


Fig.12

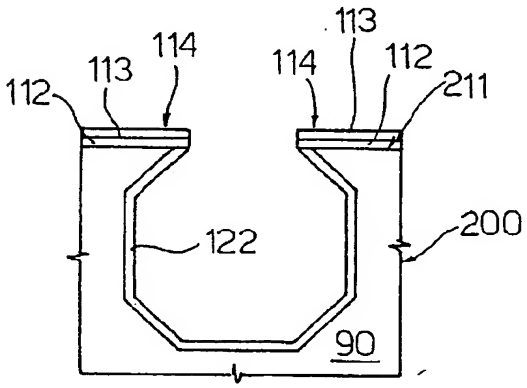


Fig.13

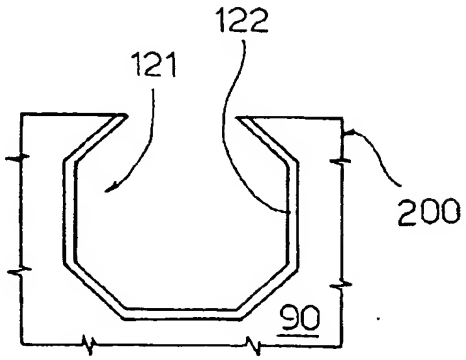
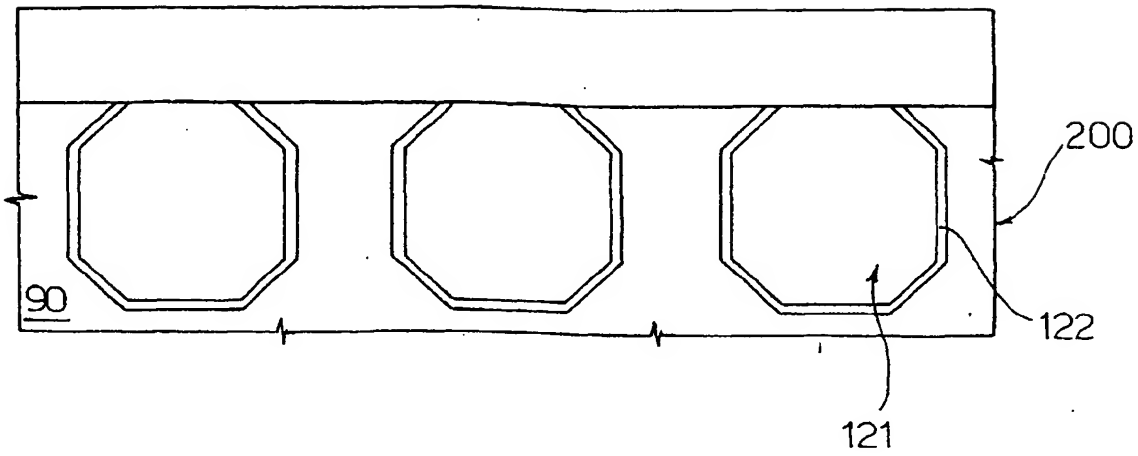


Fig.14

Fig.15



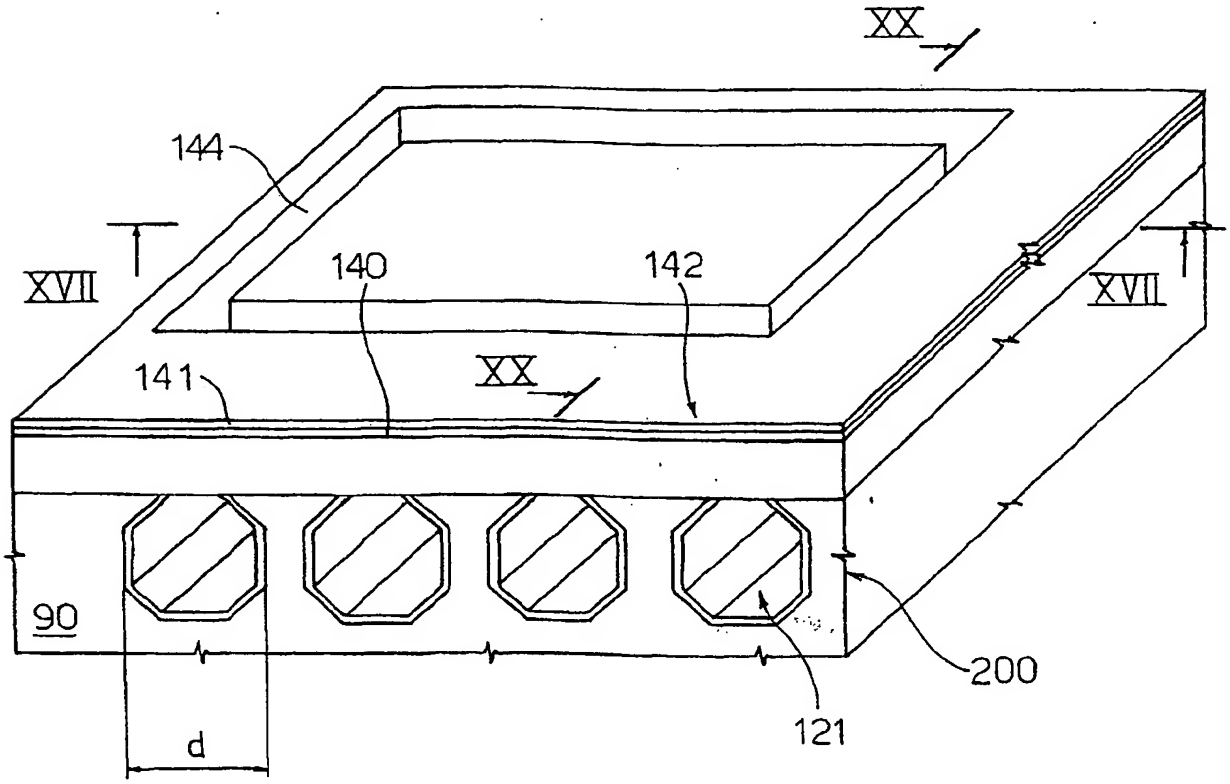


Fig.16

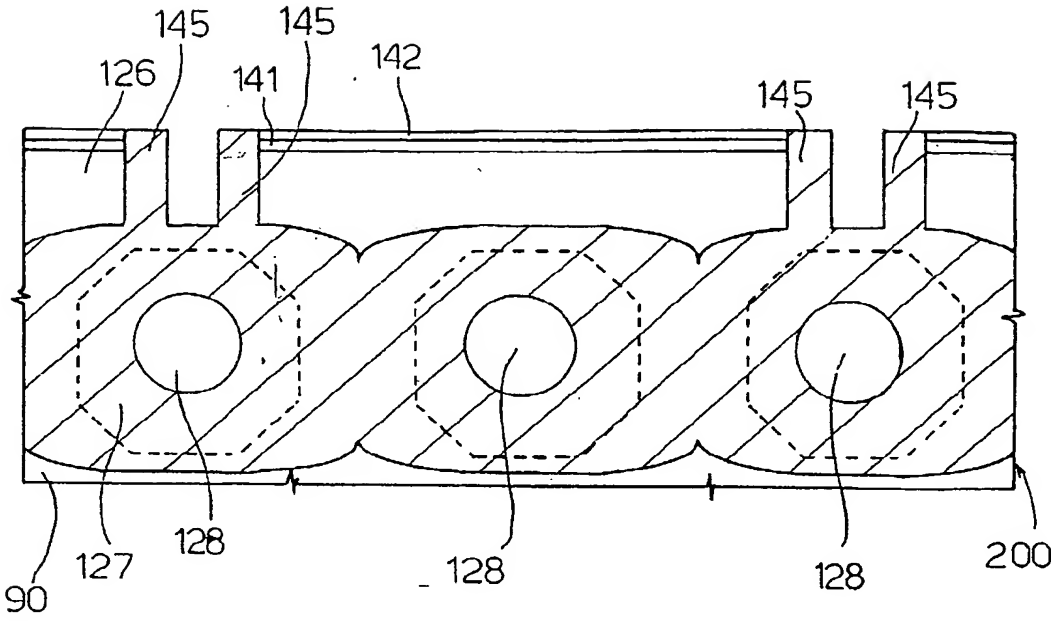

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Fig.18

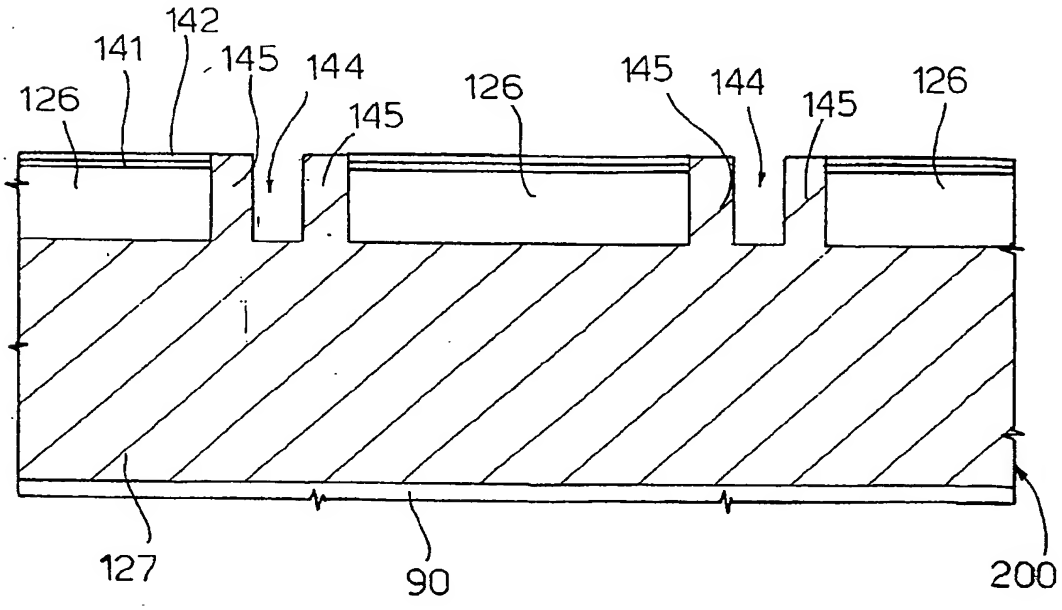
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Fig.19

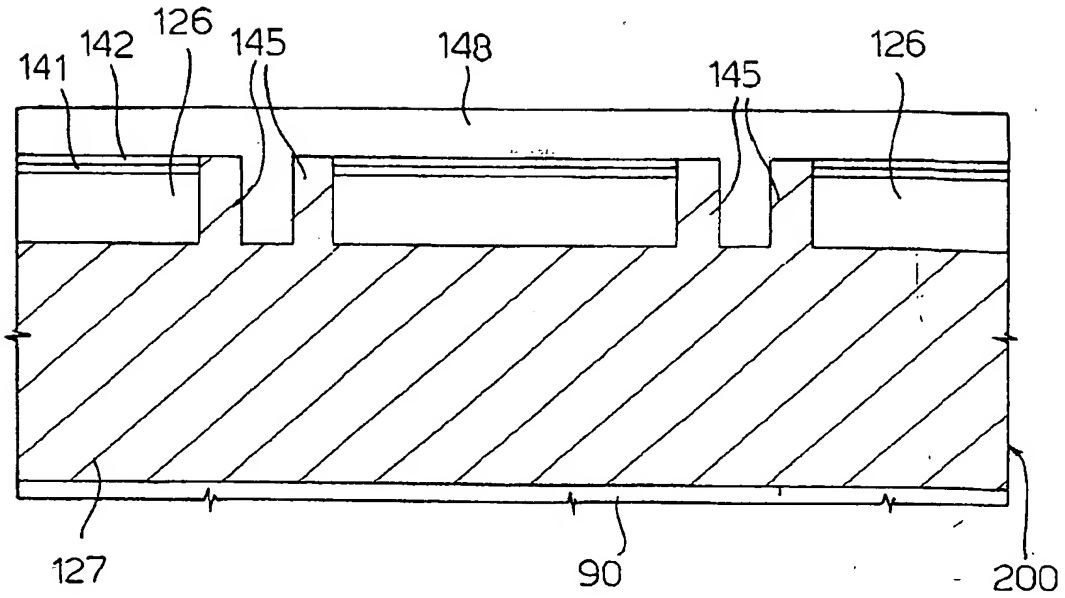
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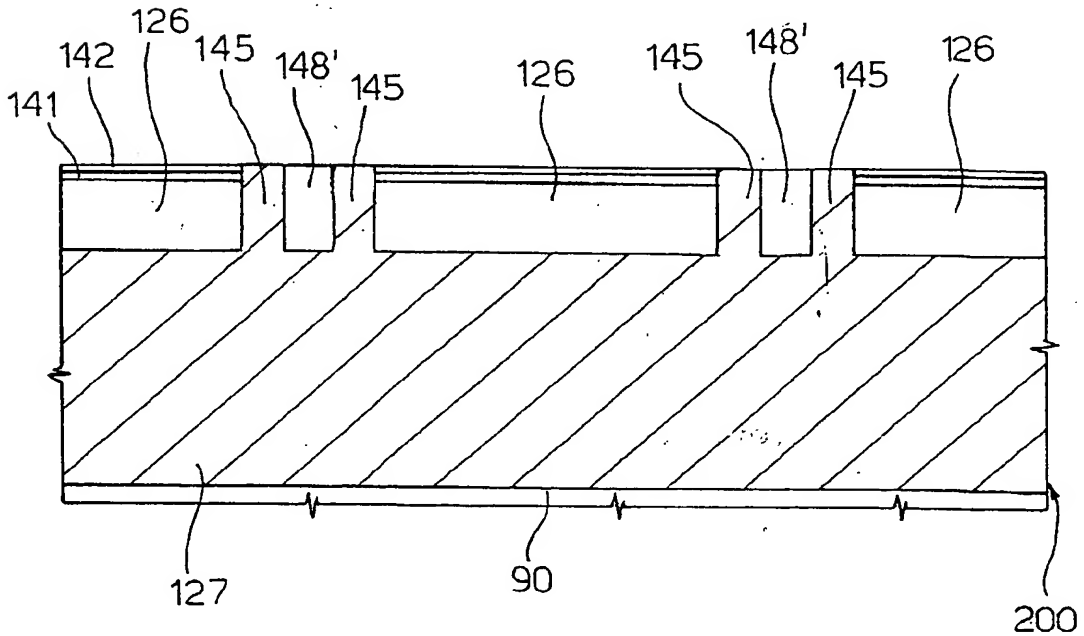
Fig.20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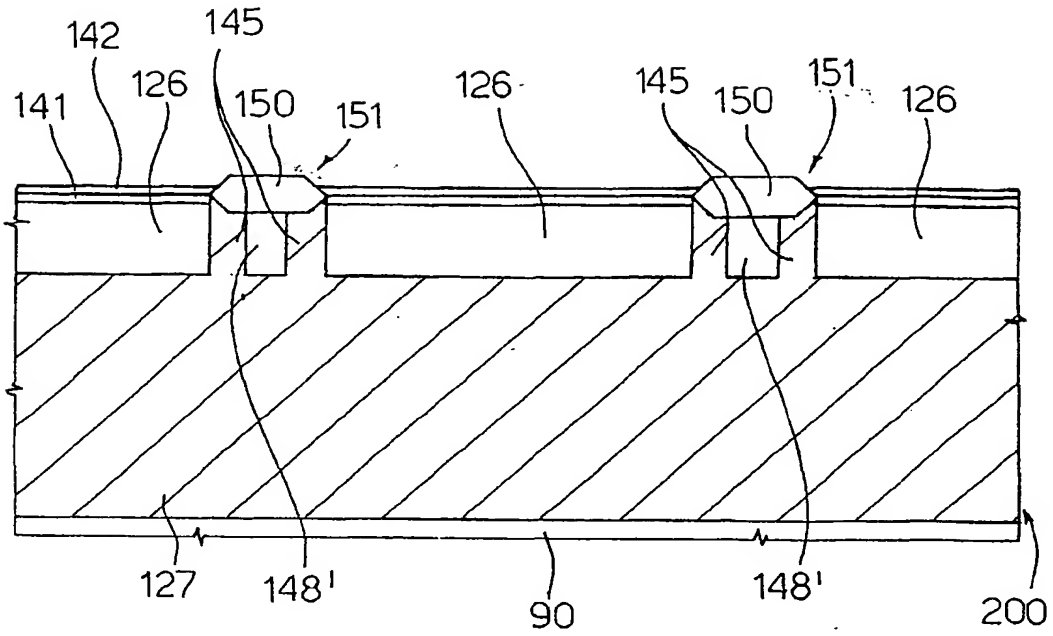
148'
145
126
145
148'
145
126
127
90
200

Fig.21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141
126
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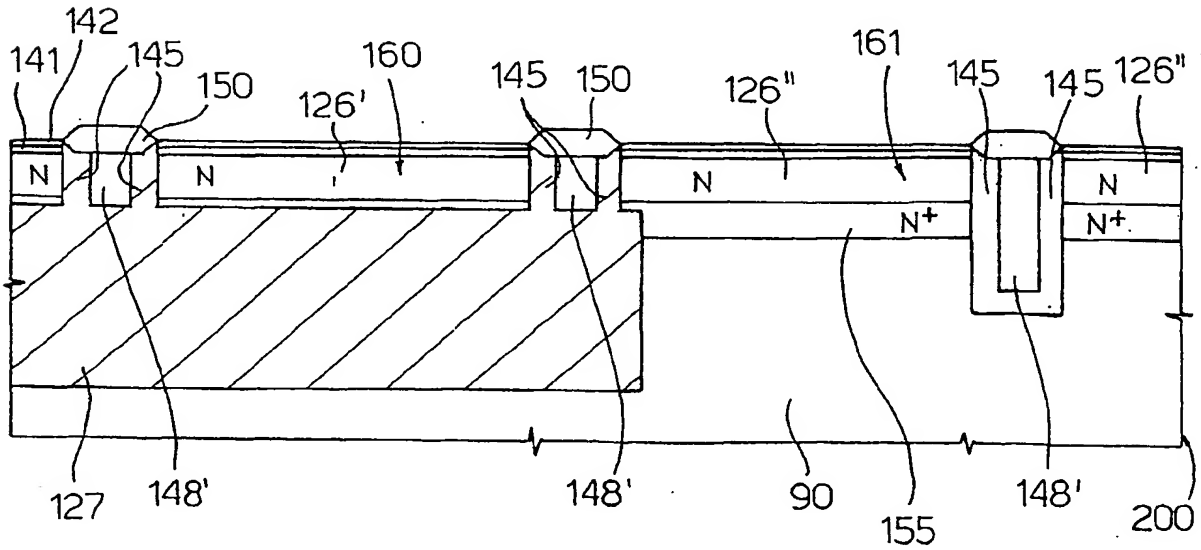
151
126
145
150
151
126
127
148'
90
148'
200

Fig.22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141
145
150
160
126'
145
150
126"
161
145
145
126"
N
N
N
N+
N
N+
127
148'
148'
90
155
148'
200

Fig.23

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0477

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 4 502 913 A (LECHATON JOHN S ET AL) 5 March 1985 (1985-03-05) * column 2, line 30 - line 66 * * column 3, line 47 - column 5, line 36; figures 1,2 * * column 5, line 45 - column 6, line 22; figures 3,4 *	14,15	H01L21/762 H01L21/20 H01L21/763
A		1,2,5, 9-11,13	
X	US 4 685 198 A (KAWAKITA KENJI ET AL) 11 August 1987 (1987-08-11) * column 4, line 26 - column 5, line 50; figures 2A-2J * * column 5, line 53 - column 6, line 15; figures 3A-3E * * column 6, line 18 - line 56; figures 4A-4J *	14	
A		1-5, 9-11,15	
X	US 5 525 824 A (HIMI HIROAKI ET AL) 11 June 1996 (1996-06-11) * column 4, line 20 - column 5, line 45; figures 1,7 *	15-17	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
X	EP 0 615 286 A (NIPPON DENSO CO) 14 September 1994 (1994-09-14) * column 2, line 49 - column 4, line 1; figures 1-5 *	14,15	
D,A	EP 0 929 095 A (ST MICROELECTRONICS SRL) 14 July 1999 (1999-07-14) * column 2, line 26 - line 38; figures 1-12 *	1,2,5,11	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	16 December 1999	Klopfenstein, P

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16-12-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4502913 A	05-03-1985	EP 0098374 A	18-01-1984
		JP 1496881 C	16-05-1989
		JP 59008346 A	17-01-1984
		JP 63047337 B	21-09-1988
		US 4661832 A	28-04-1987
US 4685198 A	11-08-1987	NONE	
US 5525824 A	11-06-1996	JP 7135248 A	23-05-1995
		US 5650354 A	22-07-1997
EP 0615286 A	14-09-1994	JP 6268054 A	22-09-1994
		US 5449946 A	12-09-1995
EP 0929095 A	14-07-1999	NONE	

EPO FORM P0459

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